ISO9002 Certified SCI Quality System

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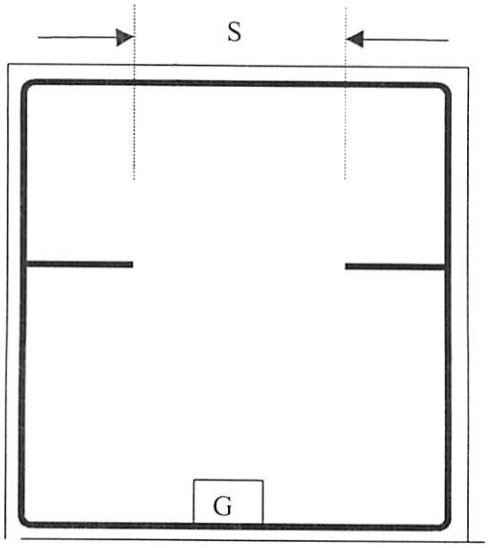
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

HEX 3 55V N-CHANNEL GEN 5



GATE 20 X 25 MILS ; SOURCE CONNECTION CENTRALLY BETWEEN INDICATOR LINES : 77 MILS

Topside Metal: Al
Backside: CrNiAg
Backside Potential: Drain
Mask Ref: Gen 5
Bond Pads (Mils): See Avove

APPROVED BY:	**DIE SIZE (Mils): 134 x 150**	**DATE: 1/24/02**
MFG: Internat'l Rect	**THICKNESS:**	**P/N: IRFC048**

DG 10.1.2
Rev A 3-4-99